MEMORY STACK ARCHITECTURE FOR REDUCED TLB MISSES

ABSTRACT OF THE DISCLOSURE

One embodiment disclosed relates to a computer system. The computer system includes a microprocessor, an operating system, and a memory system. The microprocessor includes a register stack and a register stack engine (RSE), and the operating system includes a kernel. The memory system is configured to have a single memory page that includes both a kernel stack and an RSE stack. The memory system may be further configured such that the kernel stack and the RSE stack grow in opposite directions and such that a uarea data structure is located between those two stacks.